

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In Re PATENT APPLICATION of:

Anthony Correale, Jr. et al.

Appin. No.: Unknown

Art Unit:

Filed: herewith

Examiner: Unknown

For: METHOD AND PROGRAM PRODUCT  
OF LEVEL CONVERTER  
OPTIMIZATION

**INFORMATION DISCLOSURE STATEMENT**

Mail Stop PATENT APPLICATION  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

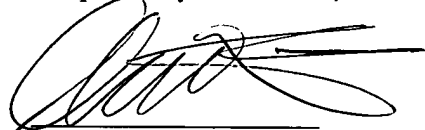
Sir,

Pursuant to the duty of disclosure under 37 C.F.R. §1.56, submitted herewith is an Information Disclosure Statement (IDS) including a Form PTO-1449 and a copy of four (4) non-patent publication. Pursuant to a Pre-OG Notice dated July 11, 2003 waiving requirement for copies of U.S. Patents and Published Applications, copies of Patents and Published Applications cited on the PTO-1449 are not included.

Since this IDS is being submitted with the application and prior to a first office action, no certification or fee is believed required, and the requirements of 37 C.F.R. §§1.97 and 1.98 are deemed to be fully met as to all documents submitted. Consideration of the submitted documents is respectfully requested.

November 24, 2003  
(Date)

Respectfully Submitted,



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U.S. PATENT DOCUMENTS

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Substitute for form 1449B/PTO  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (use as many sheets as necessary)			<b>Complete if Known</b>		
			Application Number		
			Filing Date		
			First Named Inventor	Correale, Jr. et al.	
			Art Unit		
			Examiner Name		
Sheet	2	of	2	Attorney Docket Number	YOR920030359US1

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		LACKEY ET AL., Managing power and performance for System-on-Chip designs using Voltage Islands, Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design, 11/11/2002, Page(s) 195-202	
		USAMI ET AL., CLUSTERED VOLTAGE SCALING TECHNIQUES FOR LOW-POWER DESIGN, International Symposium on Low-Power Electronic Design, 4/1/1995, Page(s) 3-8, Publisher: ACM Press	
		USAMI ET AL., AUTOMATED LOW-POWER TECHNIQUE EXPLOITING MULTIPLE SUPPLY VOLTAGES APPLIED TO A MEDIA PROCESSOR, IEEE Journal of Solid-State Circuits, 3/1/1998, Page(s) 463-472, Volume 33, Number 3	
		YEH ET AL., LAYOUT TECHNIQUES SUPPORTING THE USE OF DUAL SUPPLY VOLTAGES FOR CELL-BASED DESIGNS, Proc. ACM/IEEE Design Auto. Conf., 6/1/1999, Page(s) 62-67	

Examiner Signature		Date Considered	
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\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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